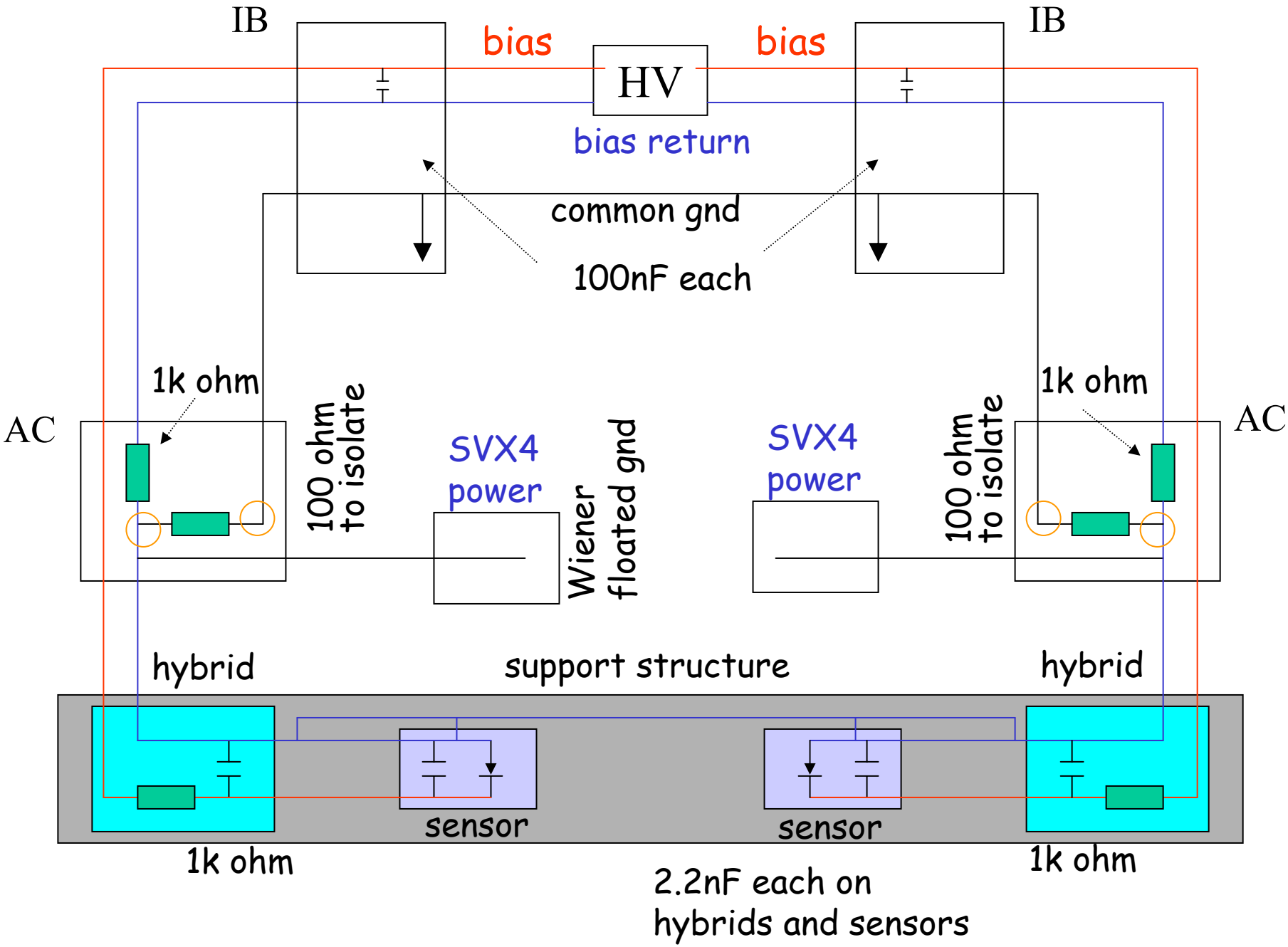
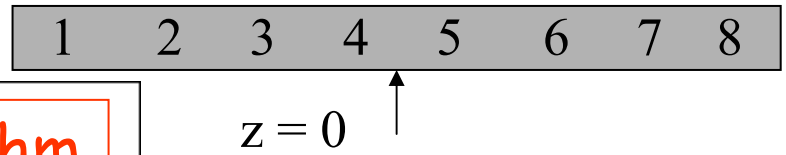
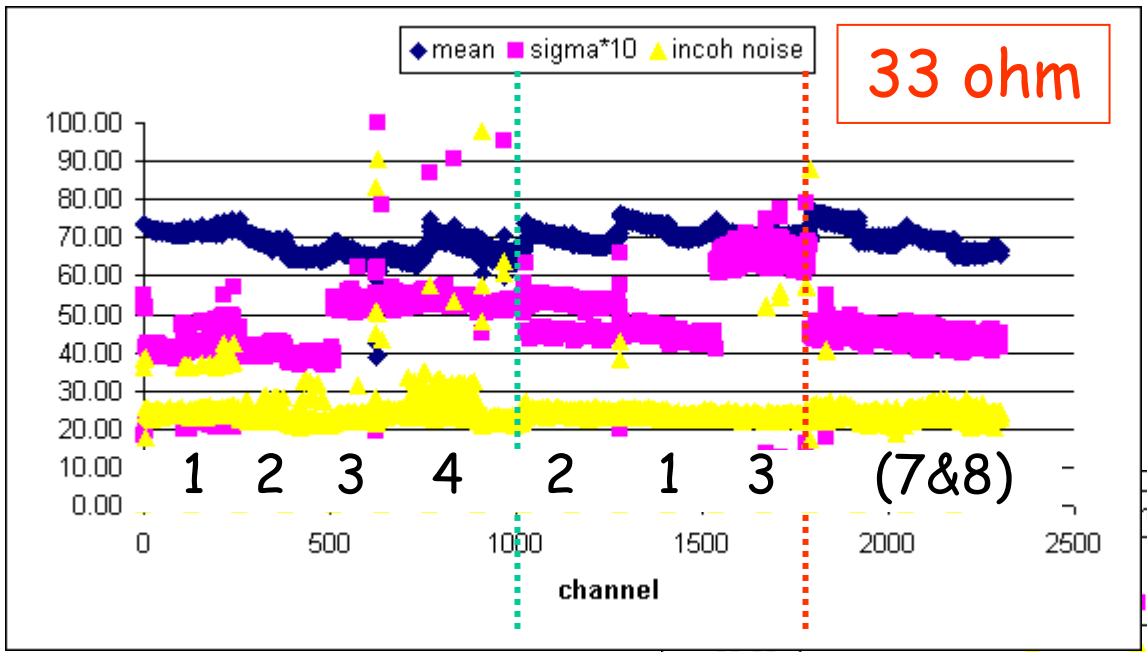
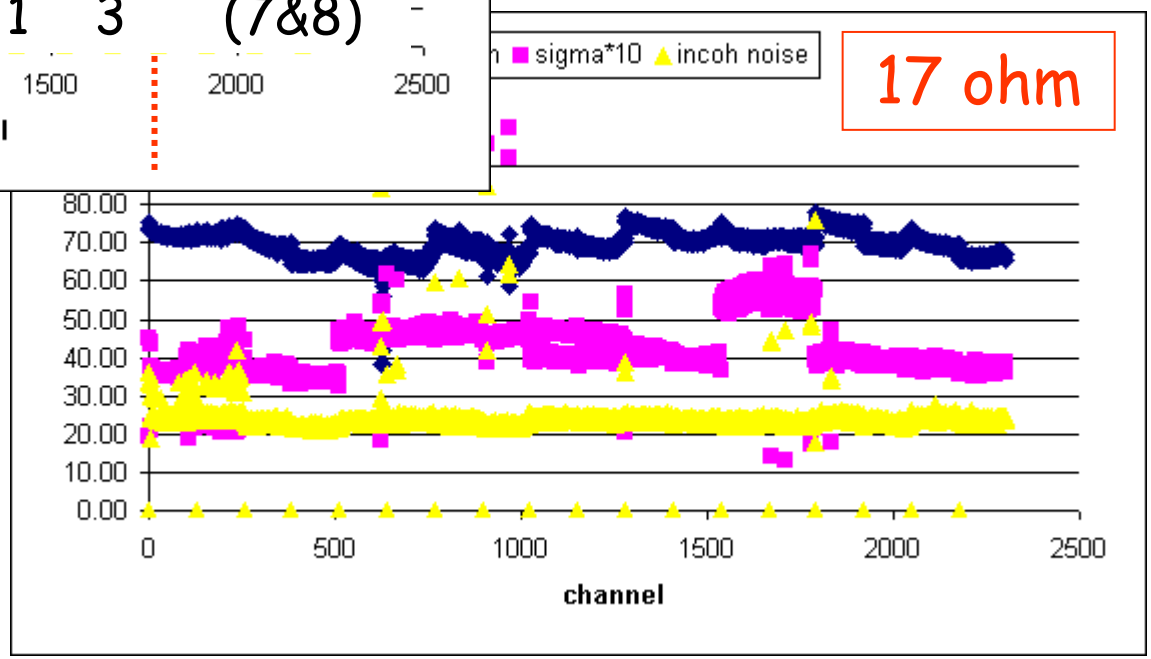

IB
bias
HV
bias
IB
bias return
common gnd
100nF each
1k ohm
AC
100 ohm to isolate
SVX4 power
Wiener floated gnd
SVX4 power
100 ohm to isolate
1k ohm
AC
hybrid
support structure
hybrid
sensor
sensor
1k ohm
1k ohm
2.2nF each on hybrids and sensors

Resistor across isolated and non-isolated GND

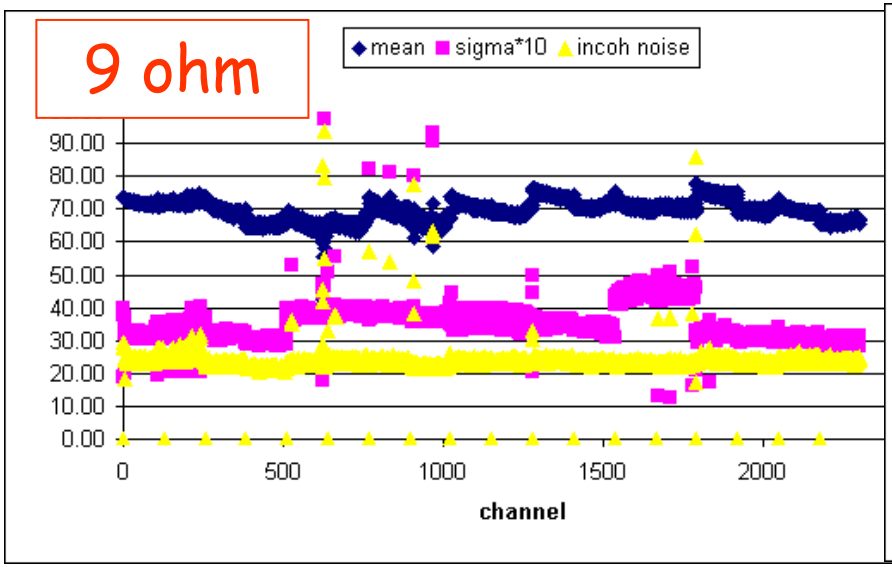


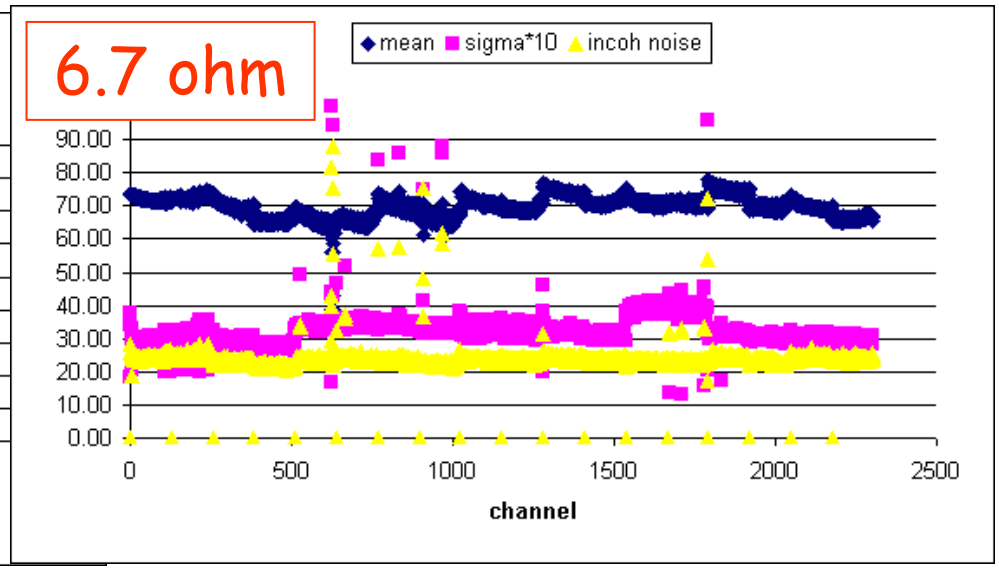


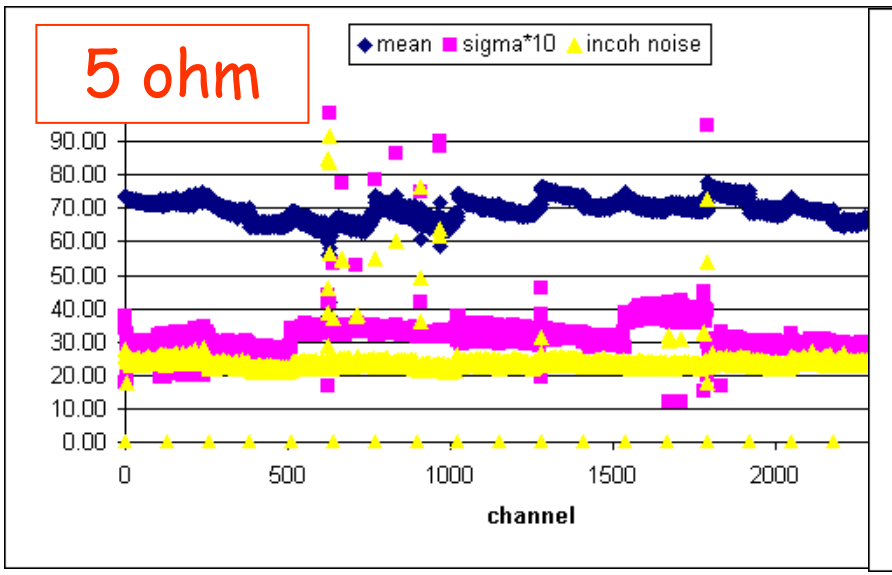
BW=4, HV=40V

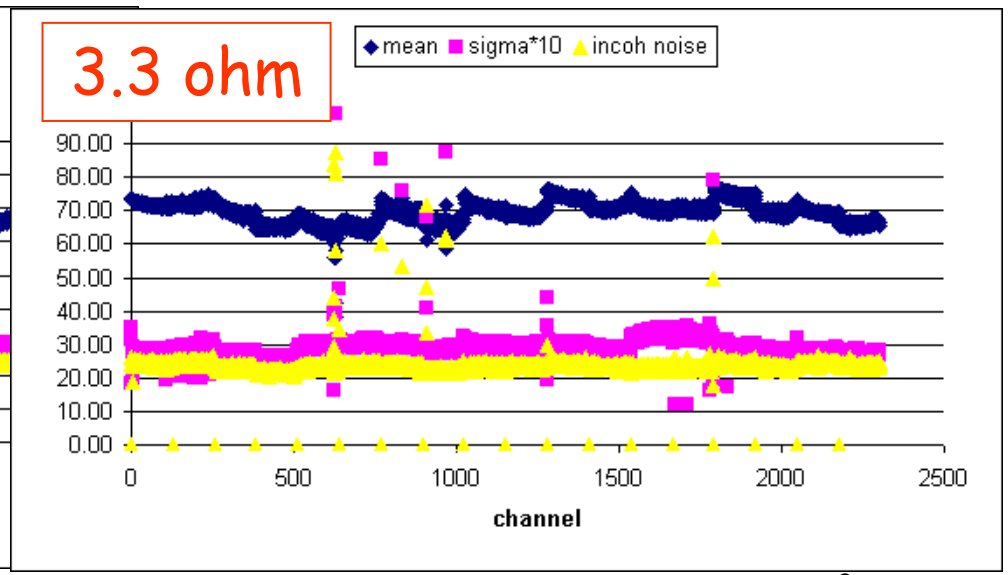


Smaller resistor

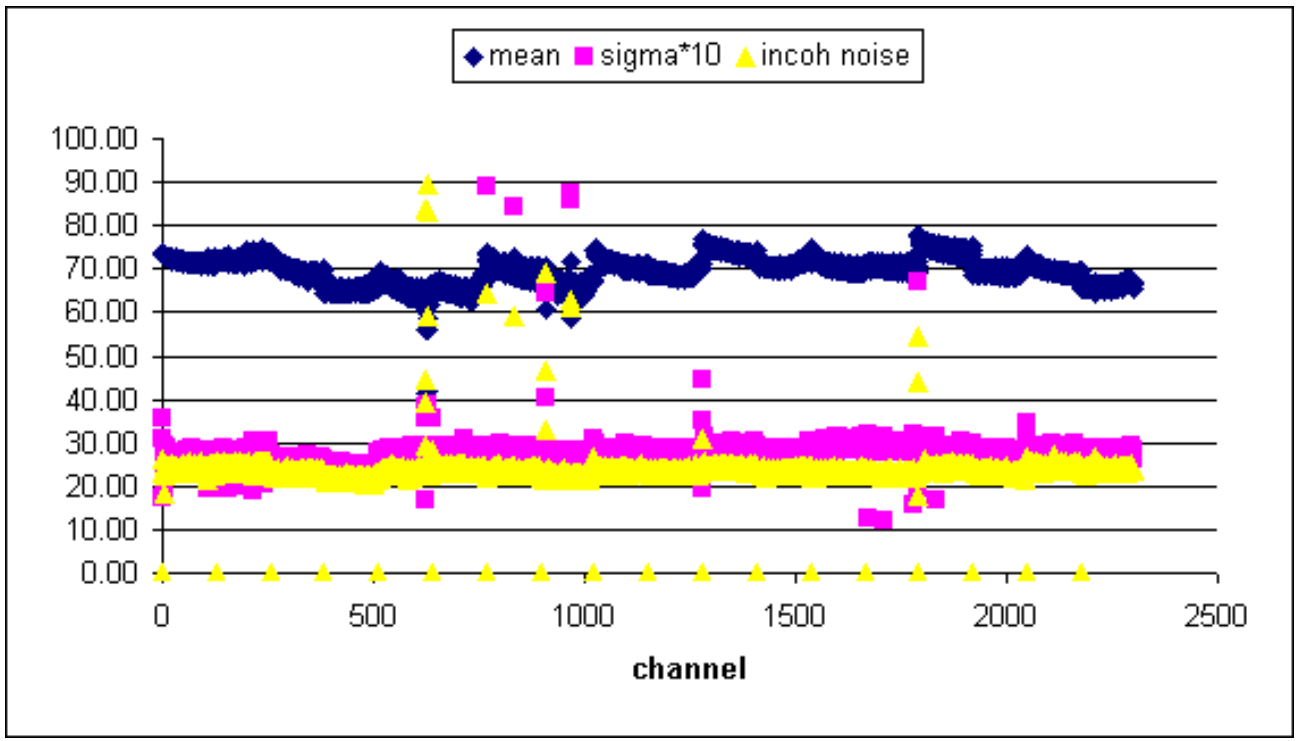






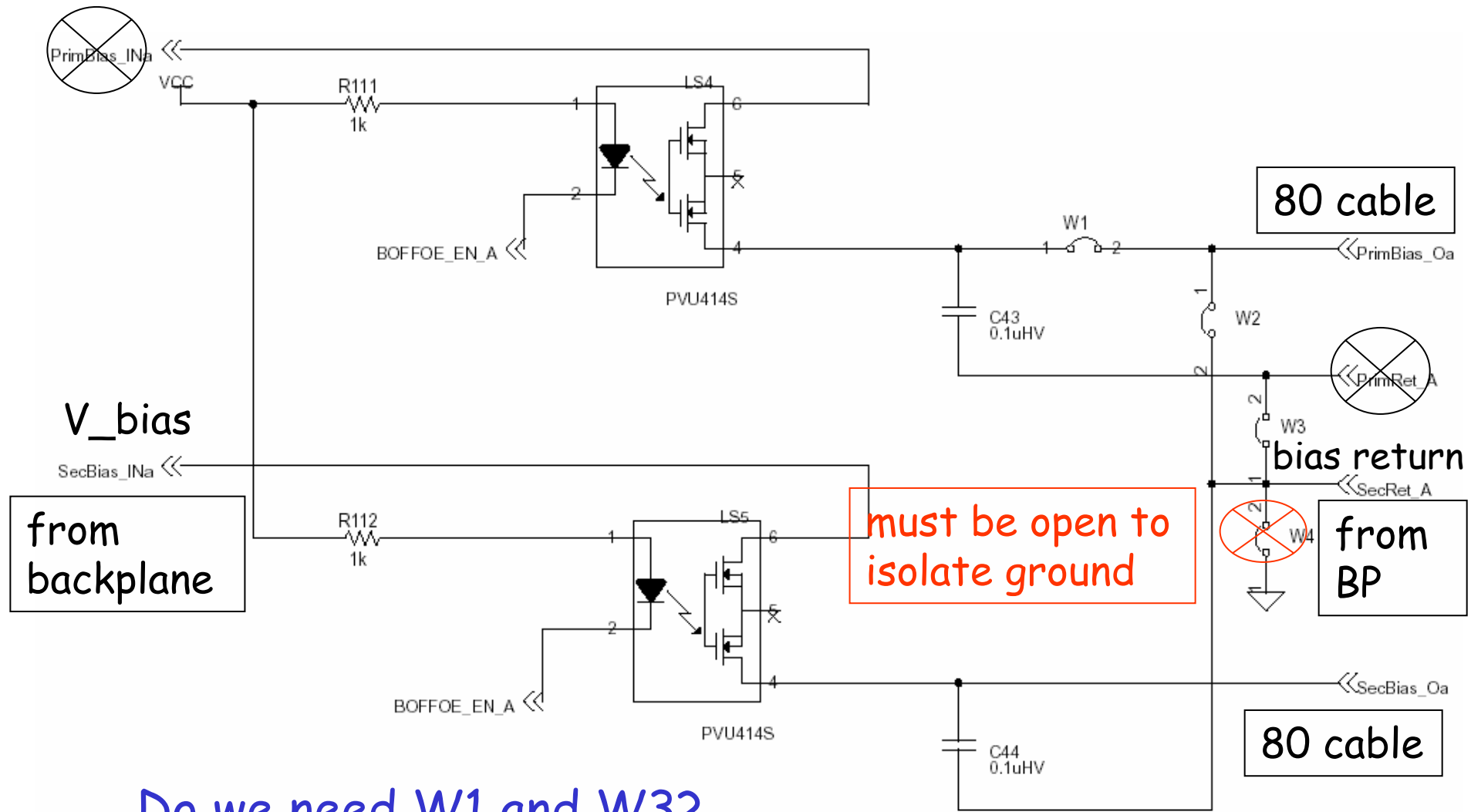


And shorted…



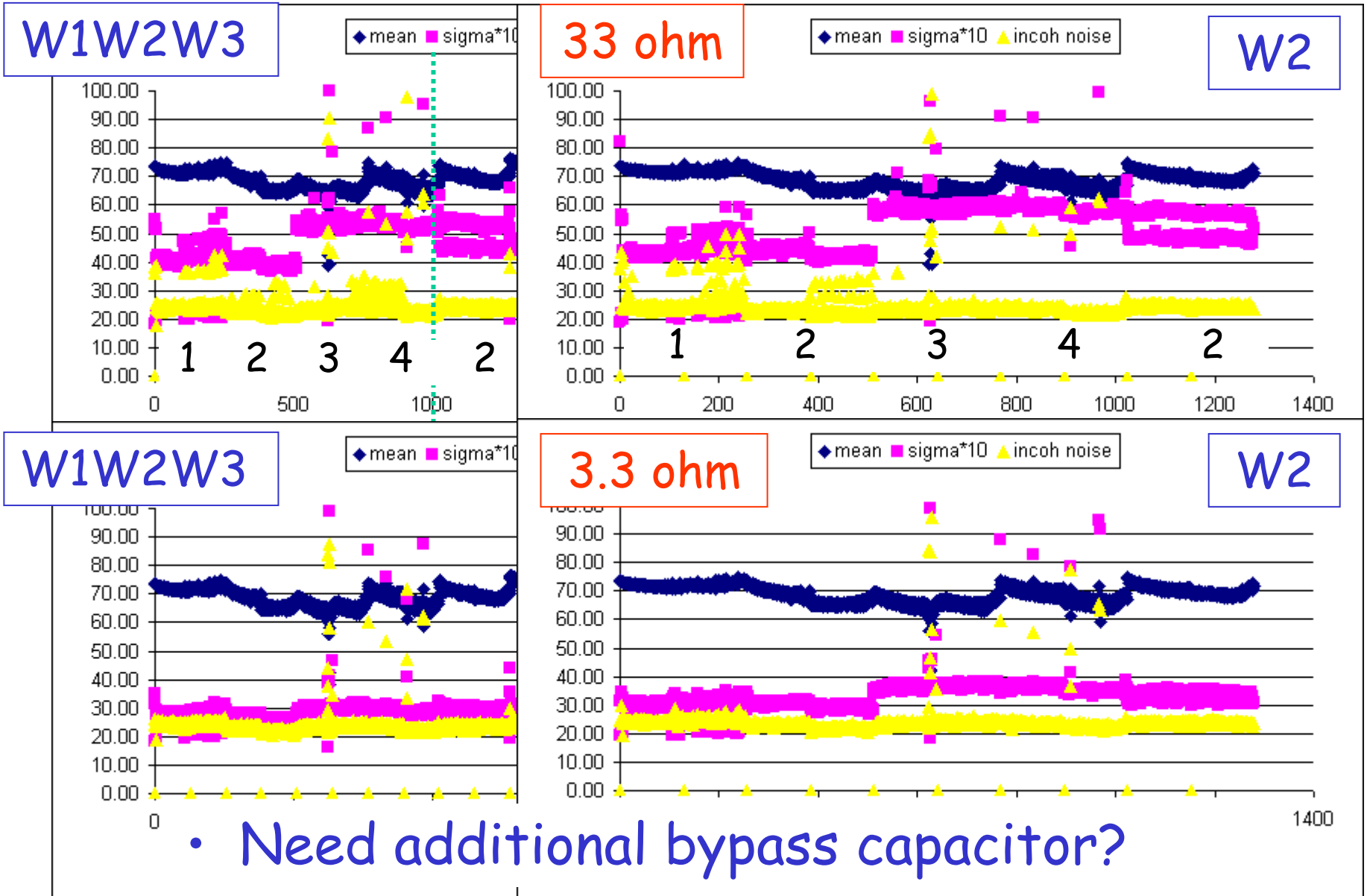
- No optimum point – smaller the better
- Potential difference seems to create current
  - but we have to isolate them

Bias configuration in IB



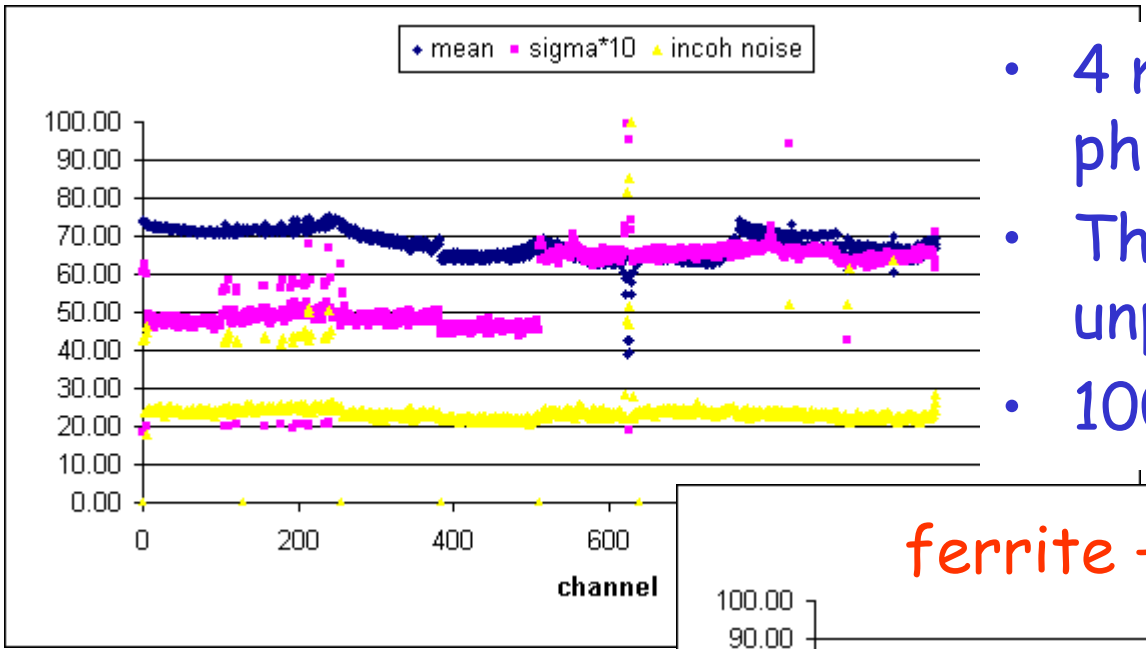
Do we need W1 and W3?

W1&W2&W3 (default) vs W2

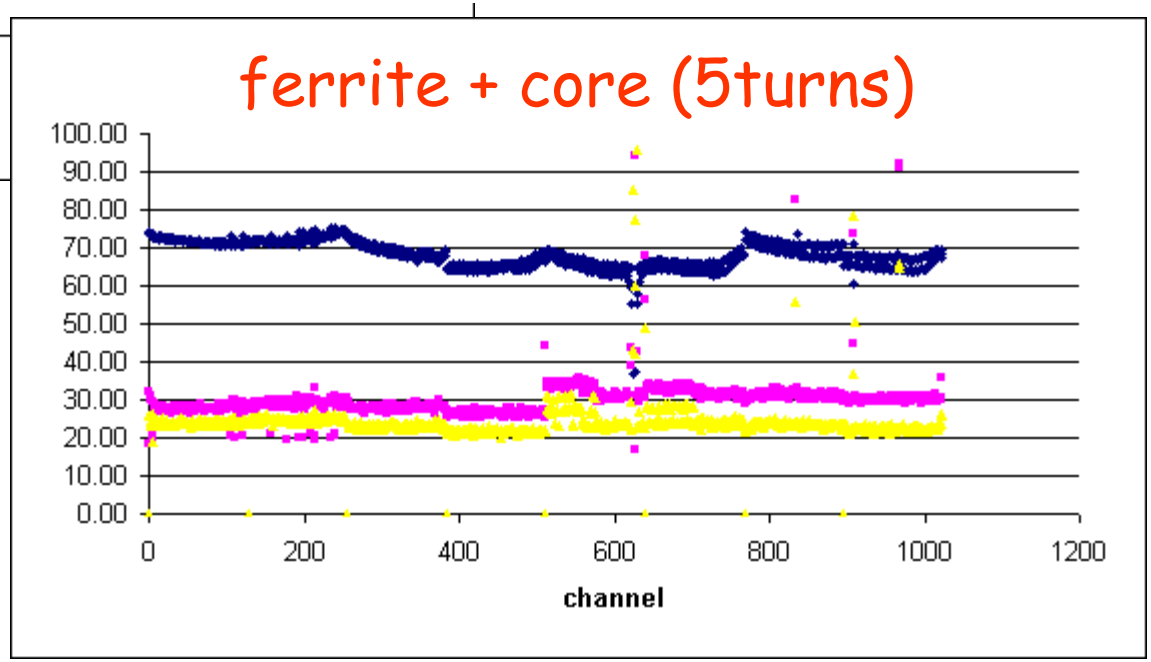


- Need additional bypass capacitor?

Putting ferrite onto power lines

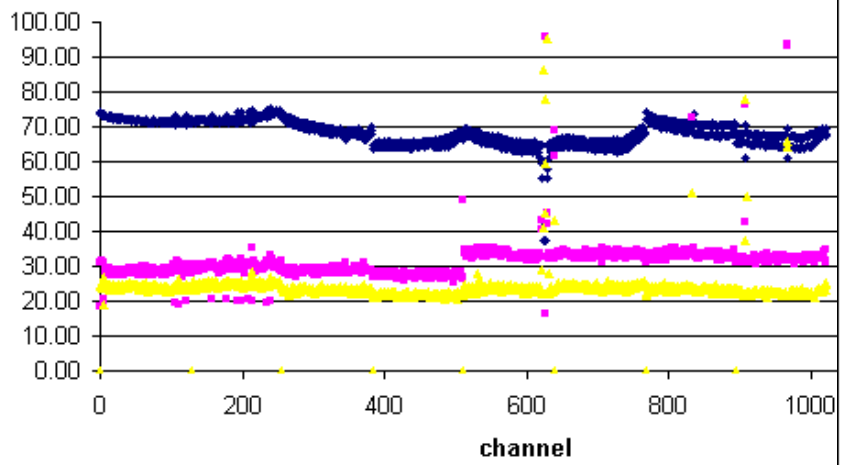


- 4 modules in the same phi sector
- The other power lines unplugged
- 100 ohm isolation

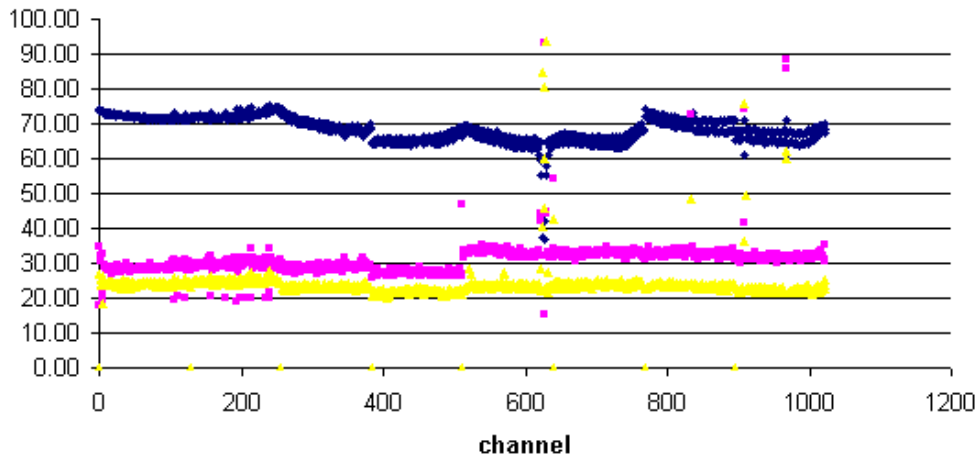


Different ferrites

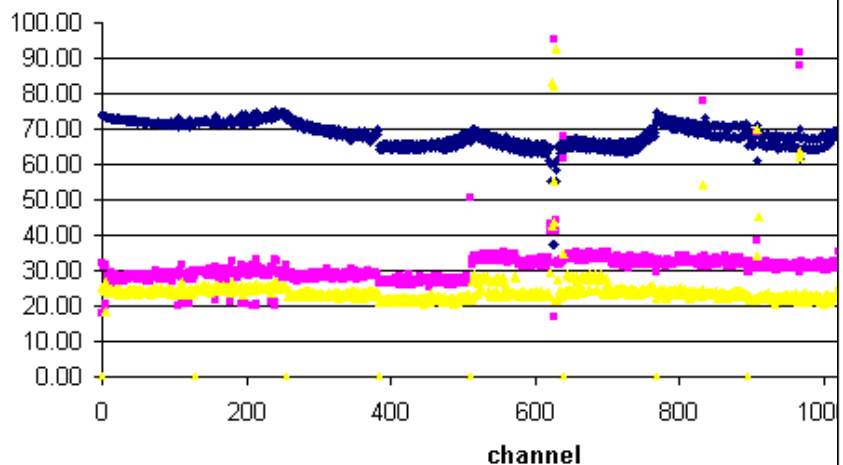
core (5 turns)



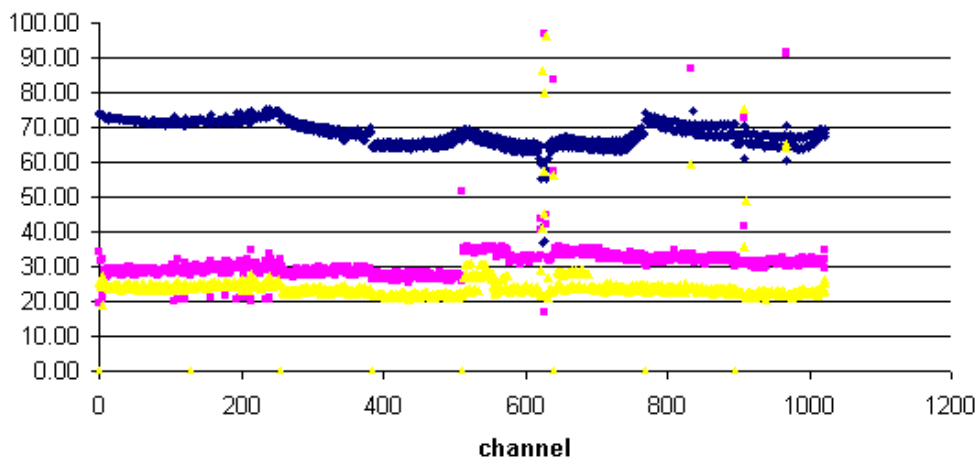
ferrite (5 turns)



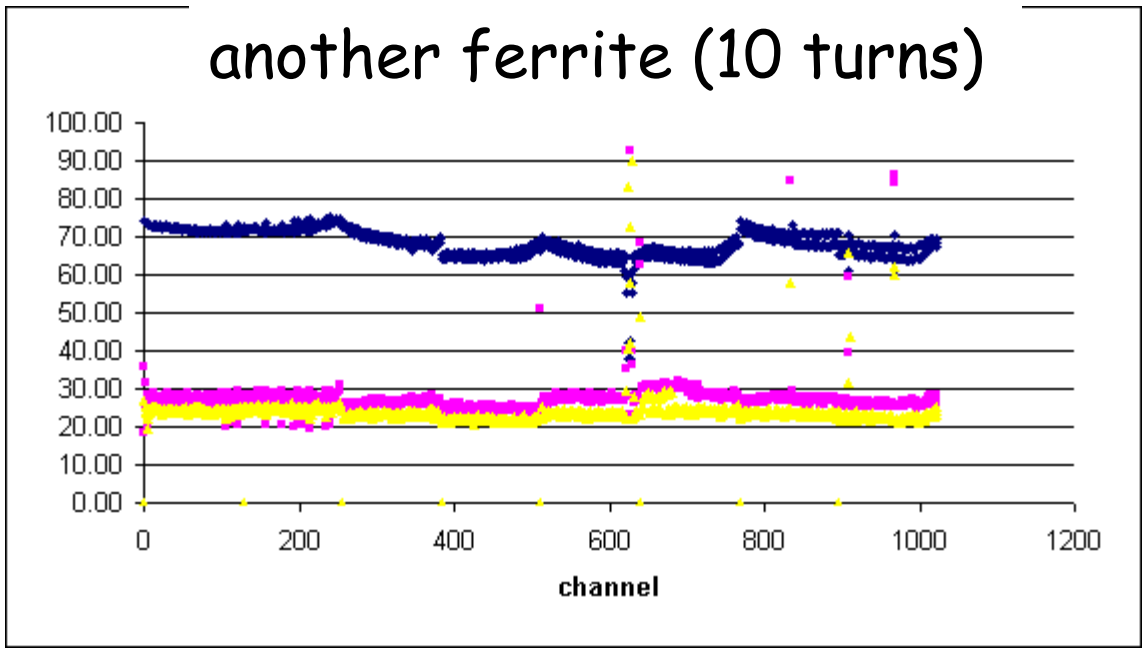
another ferrite (5 turns)



another ferrite (10 turns)



Something out of control…



- The same setup with the last plot in previous page, but the noise is much small…

Summary and Plan

- We now have much better understanding of the source of noise – it is pickup from the power line for SVX4
  - this may explain the reason of having different noise between north and south
  - not a good solution, but… we may be able to survive with RTPS even if we can't fix the problem completely: the pickup will be really coherent and uniform across a chip
- Possible options (can be studied in 100% test)
  - ferrite (core) with shield cage
  - shielding of whole power lines
  - others